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SPECIFICATION

CUSTOMER : _____

MODULE NO.: WDX0006-TGH-#00

APPROVED BY: **(FOR CUSTOMER USE ONLY)**	**PCB VERSION: DATA:**

SALES BY	APPROVED BY	CHECKED BY	PREPARED BY

VERSION	DATE	REVISED PAGE NO.	SUMMARY
A	2010.02.26	8	Add drawing

Winstar Display Co., LTD
華凌光電股份有限公司

MODLE NO：

RECORDS OF REVISION

DOC. FIRST ISSUE

VERSION	DATE	REVISED PAGE NO.	**SUMMARY**
0	2007.05.07		First issue
A	2010.02.26	8	Add drawing

Contents

1.Module Classification Information

W DX 0006 – T G H – #00
① ② ③ ⑤ ⑥⑦ ⑧

① Brand：WINSTAR DISPLAY CORPORATION

② Custom：D

③ Display Type：H→ Character Type ; G→ Graphic Type;

N → LCD Display; X→ TAB Type

④ Model serials no.0000 - ZZZZ

⑤ Backlight Type：

N→Without backlight	T→LED, White
B→EL, Blue green	A→LED, Amber
D→EL, Green	R→LED, Red
W→EL, White	O→LED, Orange
F→CCFL, White	G→LED, Green
Y→LED, Yellow Green	

⑥ LCD Mode：

B→TN Positive, Gray	T→FSTN Negative
N→TN Negative,	
G→STN Positive, Gray	
Y→STN Positive, Yellow Green	
M→STN Negative, Blue	
F→FSTN Positive	

⑦ LCD Polarizer Type/ Temperature range/ View direction

A→Reflective, N.T, 6:00	H→Transflective, W.T,6:00
D→Reflective, N.T, 12:00	K→Transflective, W.T,12:00
G→Reflective, W. T, 6:00	C→Transmissive, N.T,6:00
J→Reflective, W. T, 12:00	F→Transmissive, N.T,12:00
B→Transflective, N.T,6:00	I→Transmissive, W. T, 6:00
E→Transflective, N.T.12:00	L→Transmissive, W.T,12:00

⑧ Special Code 00:Sales Code (LED 4Dice)

#: Fit in with the ROHS directives and regulations

2.Precautions in Use of LCD Module

(1)Avoid applying excessive shocks to the module or making any alterations or modifications to it.

(2)Don't make extra holes on the printed circuit board, modify its shape or change the components of LCD Module.

(3)Don't disassemble the LCM.

(4)Don't operate it above the absolute maximum rating.

(5)Don't drop, bend or twist LCM.

(6)Soldering: only to the I/O terminals.

(7)Storage: please storage in anti-static electricity container and clean environment.

3.General Specification

ITEM	STANDARD VALUE	UNIT
Number of dots	96x64	dots
Outline dimension	417.2(W)x 38.95(H)x 8.5max(T)	mm
View area	36.52(W) x 25.35(H)	mm
Active area	33.52(W)x 22.35(H)	mm
Dot size	0.329(W)x 0.329(H)	mm
Dot pitch	0.349(W)x 0.349(H)	mm
LCD type	STN, positive, Transflective,	
View direction	6 o'clock	
Backlight	LED, White	

4.Absolute Maximum Ratings

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Operating Temperature	T_{OP}	-20	—	+70	℃
Storage Temperature	T_{ST}	-30	—	+80	℃

5.Electrical Characteristics

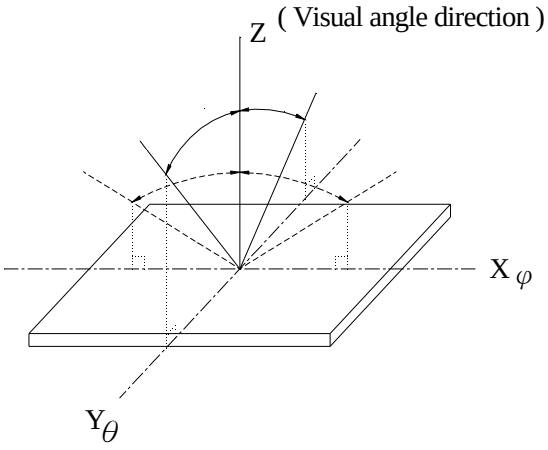
ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Logic Voltage	V_{DD}-V_{SS}	—	—	3.3	—	V
Supply Voltage For LCD	Vo-V_{SS}	Ta= -20℃	—	—	—	V
		Ta= 25℃	—	9	—	V
		Ta=+70℃	—	—	—	V
Input High Volt.	V_{IH}	—				V
Input Low Volt.	V_{IL}	—				V
Output High Volt.	V_{OH}	—				V
Output Low Volt.	V_{OL}	—				V
Supply Current	I_{DD}	—		0.7		mA

6.Optical Characteristics

ITEM	SYMBAL	CONDITION	MIN	TYP	MAX	UNIT
View Angle	(V) θ	CR≧2	20	—	40	deg.
	(H) φ	CR≧2	-30	—	30	deg.
Contrast Ratio	CR	—	—	3	—	—
Response Time	T rise	—	—	200	300	ms
	T fall	—	—	150	200	ms

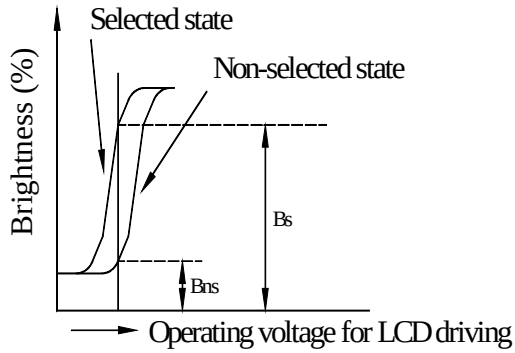
6.1 Definitions

■View Angles

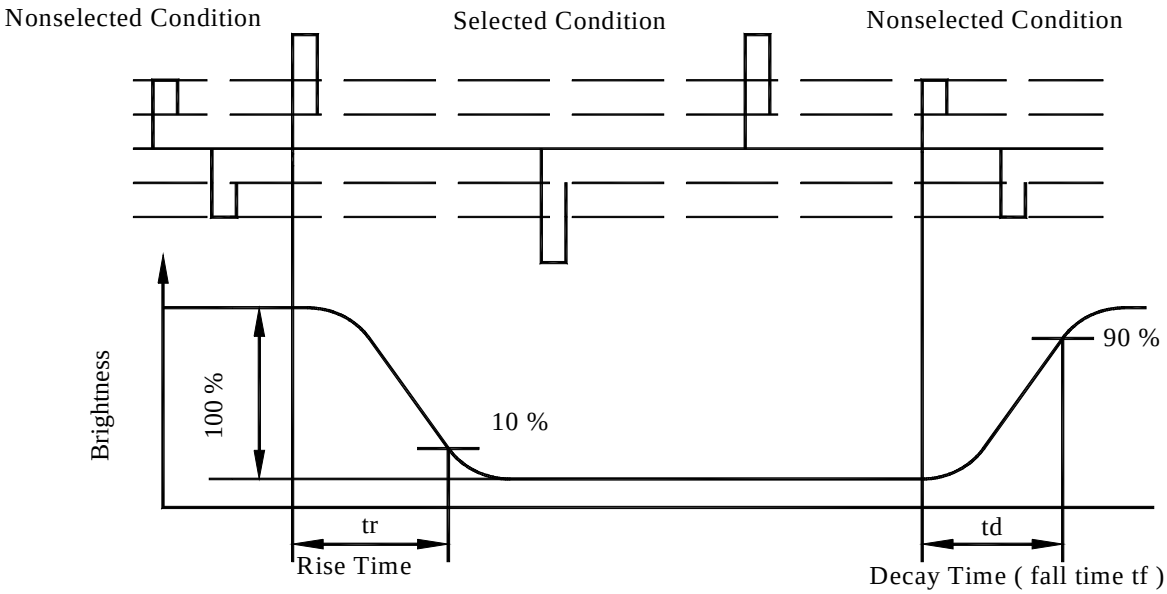


■Contrast Ratio

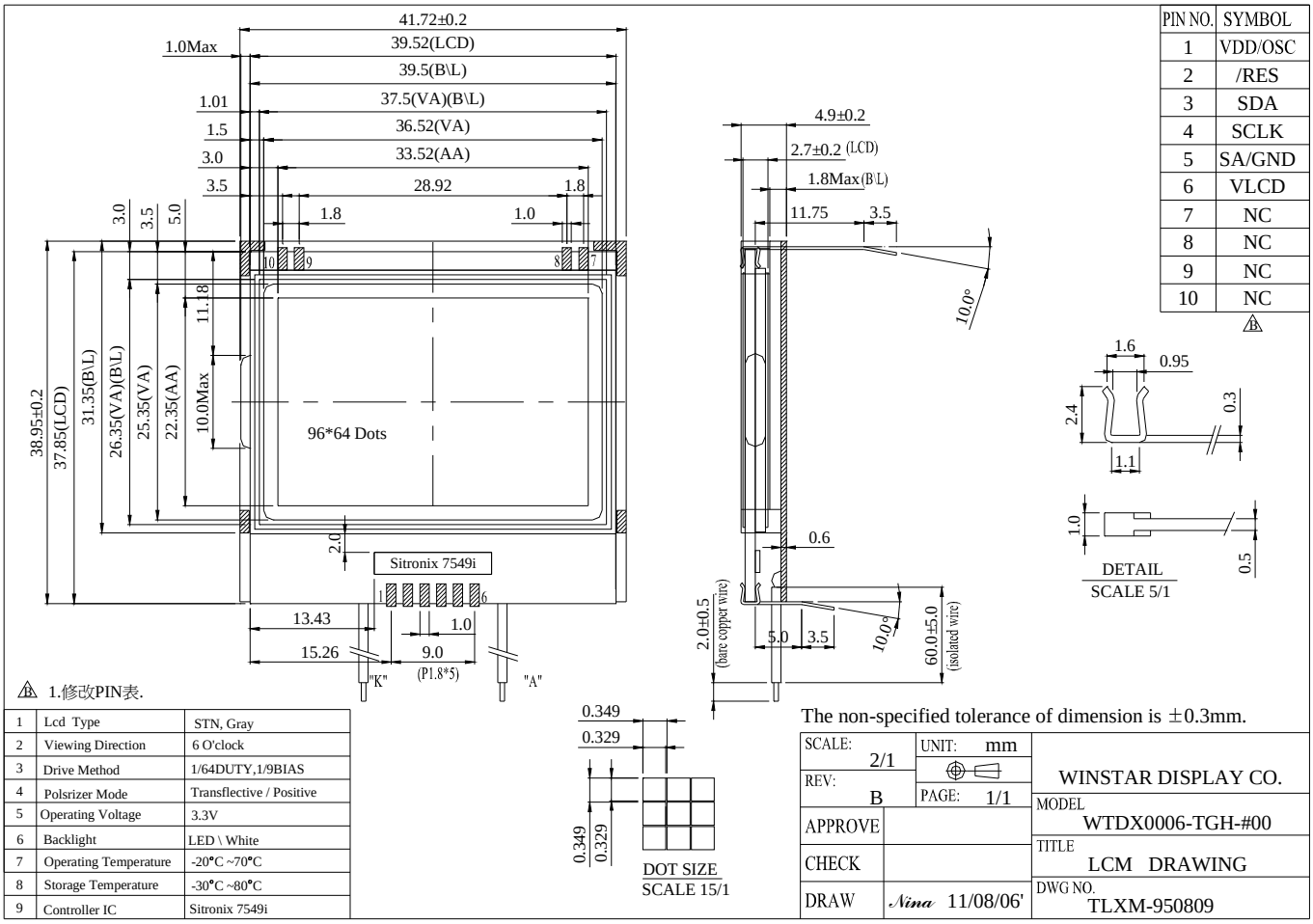
$$CR = \frac{\text{Brightness at selected state (BS)}}{\text{Brightness at non-selected state (Bns)}}$$



■Response time



7.Contour Drawing



PIN NO.	SYMBOL
1	VDD/OSC
2	/RES
3	SDA
4	SCLK
5	SA/GND
6	VLCD
7	NC
8	NC
9	NC
10	NC

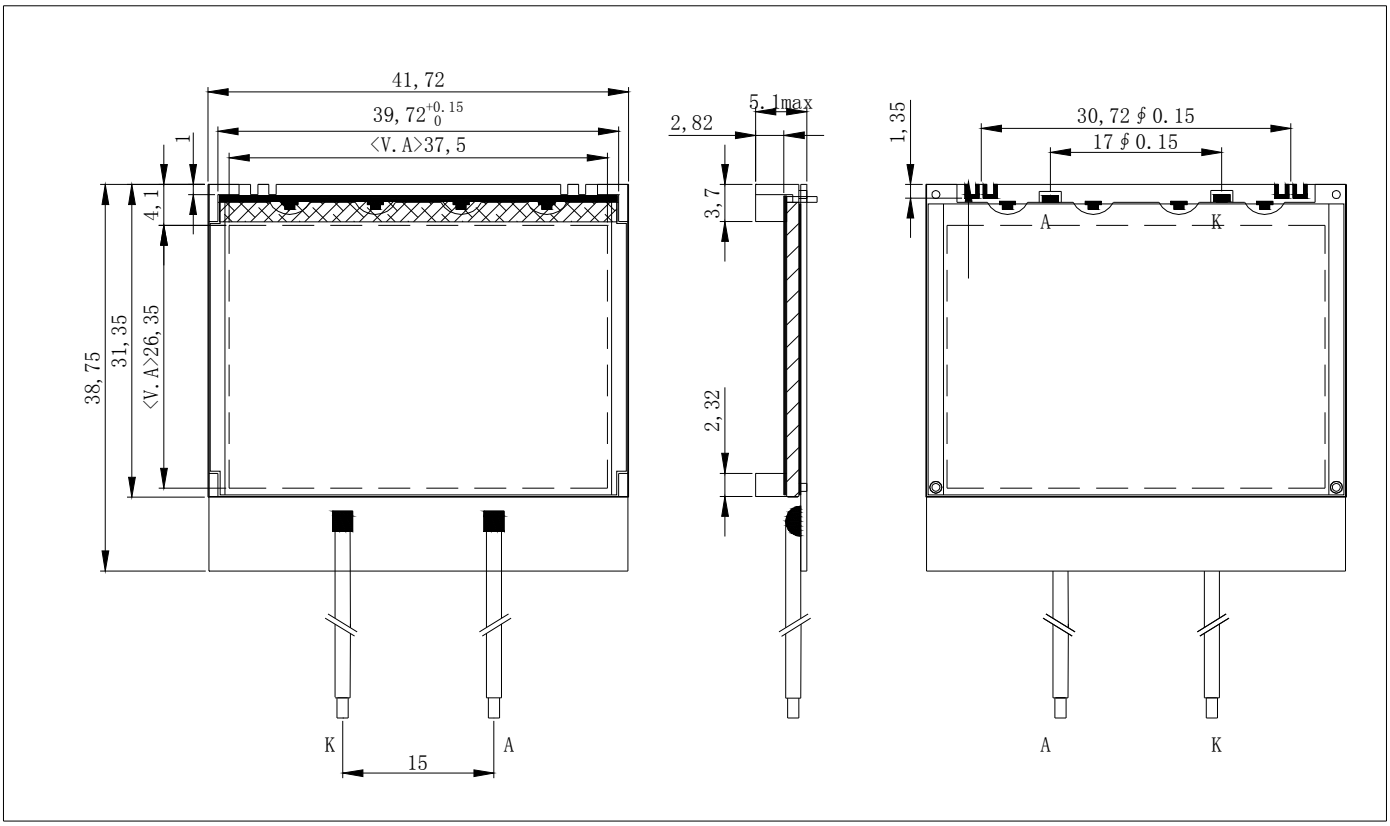
⚠B

⚠B 1.修改PIN表.

1	Lcd Type	STN, Gray
2	Viewing Direction	6 O'clock
3	Drive Method	1/64DUTY,1/9BIAS
4	Polsrizer Mode	Transflective / Positive
5	Operating Voltage	3.3V
6	Backlight	LED \ White
7	Operating Temperature	-20℃~70℃
8	Storage Temperature	-30℃~80℃
9	Controller IC	Sitronix 7549i

The non-specified tolerance of dimension is ±0.3mm.

SCALE: 2/1	UNIT: mm	WINSTAR DISPLAY CO.
REV: B	PAGE: 1/1	
APPROVE		MODEL: WTDX0006-TGH-#00
CHECK		TITLE: LCM DRAWING
DRAW	Nina 11/08/06'	DWG NO.: TLXM-950809



8.Interface Pin Function

Pin No.	Symbol	Level	Description
1	VDD/OSC	3.3V	Power supply for Logic
2	/RES	H/L	Reset
3	SDA		serial input data
4	SCLK		serial input clock
5	SA/GND	0V	Ground
6	VLCD		Scan start-up signal
7	NC		No connection
8	NC		No connection
9	NC		No connection
10	NC		No connection

9. Function Description

MICROPROCESSOR INTERFACE

Chip Select Input

There is CSB pin for chip selection. The ST7549T can interface with an MPU when CSB is "L". When CSB is “H”, these pins are set to any other combination, A0, /RD(E), and /WR(R/W) inputs are disabled and D0 to D7 are to be high impedance.

And, in case of serial interface, the internal shift register and the counter are reset.

Parallel / Serial Interface

ST7549T has five types of interface with an MPU, which are three serial and two parallel interfaces. This parallel or serial interface is determined by PS [0:2] pin as shown in table 1.

Table 1. Parallel/Serial Interface Mode

PS0	PS1	PS2	CSB	A0	State
" L "	" L "	" L "	CSB	A0	4 Pin-SPI MPU interface
" L "	" L "	" H "	CSB	" * "	3 Pin-SPI MPU interface
" L "	" H "	" L "	CSB	A0	8080-series parallel MPU interface
" L "	" H "	" H "	CSB	A0	6800-series parallel MPU interface
" H "	" H "	" H "	" * "	" * "	I^2C interface

Parallel Interface

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by PS2 as shown in table 2.

The type of data transfer is determined by signals at A0, /RD (E) and /WR(R/W) as shown in table 3.

Table 2. Microprocessor Selection for Parallel Interface

PS0	PS1	PS2	CSB	A0	/RD (E)	/WR (R/W)	DB0 to DB7	MPU bus
L	H	H	CSB	A0	E	R/W	DB0 to DB7	6800-series
L	H	L	CSB	A0	/RD	/WR	DB0 to DB7	8080-series

Table 3. Parallel Data Transfer

Common	6800-series		8080-series		Description
A0	E (/RD)	R/W (/WR)	/RD (E)	/WR (R/W)	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Register status read
L	H	L	H	L	Writes to internal register (instruction)

NOTE: When /RD (E) pin is always pulled high for 6800-series interface, it can be used CSB for enable signal. In this case, interface data is latched at the rising edge of CSB and the type of data transfer is determined by signals at A0, /WR(R/W) as in case of 6800-series mode.

Serial Interface

Serial Mode	PS0	PS1	PS2	CSB	A0
4-line SPI interface	L	L	L	CSB	Used
3-line SPI interface	L	L	H	CSB	Not Used Fix to "H"
I^2C interface	H	H	H	Not Used Fix to "H"	Not Used Fix to "H"

PS0=" L ", PS1=" L ", PS2=" L ": 4-line SPI interface

When the ST7549T is active (CSB="L"), serial data (D1) and serial clock (D0) inputs are enabled. And not active, the internal 8-bit shift register and the 3-bit counter are reset. The display data/command indication may be controlled either via software or the Register Select (A0) Pin, based on the setting of PS[2:0]. When the A0 pin is used , data is display data when A0 is high, and command data when A0 is low. When A0 is not used , the LCD Driver will receive command from MCU by default. If messages on the data pin are data rather than command, MCU should send Data direction command to control the data direction and then one more command to define the number of data bytes will be write. After these two continuous commands are sending, the following messages will be data rather than command. Serial data can be read on the rising edge of serial clock going into D0 and processed as 8-bit parallel data on the eighth serial clock. And the DDRAM column address pointer will be increased by one automatically. The next bytes after the display data string are handled as command data.

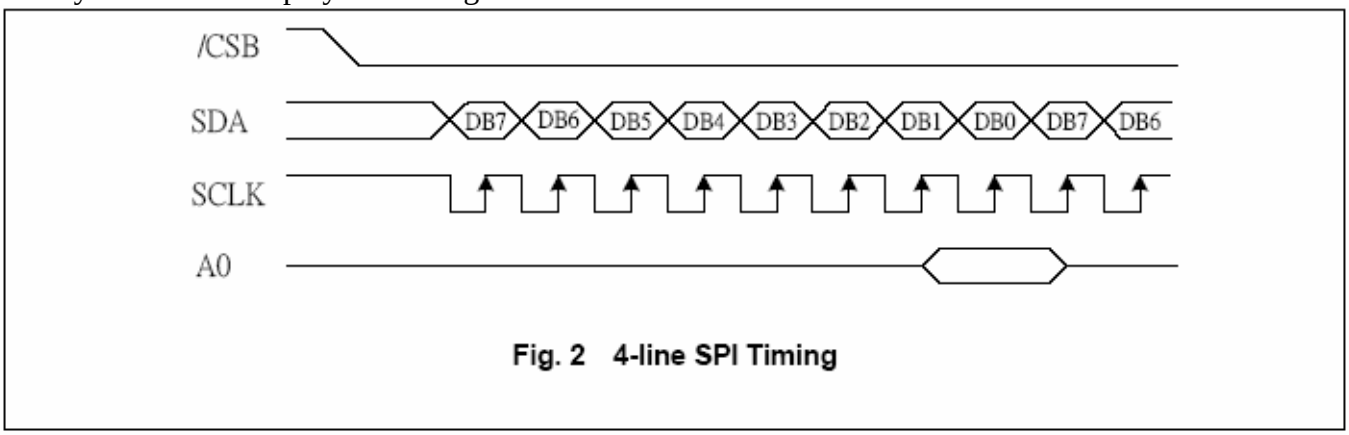


Fig. 2 4-line SPI Timing

PS0=" L ", PS1=" L ", PS2=" H ": 3-line SPI interface

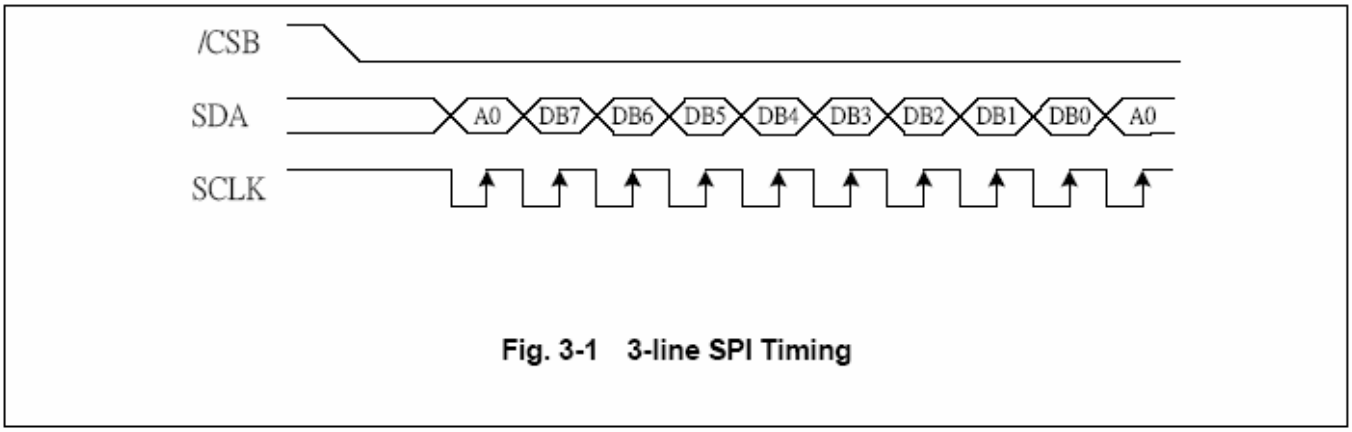


Fig. 3-1 3-line SPI Timing

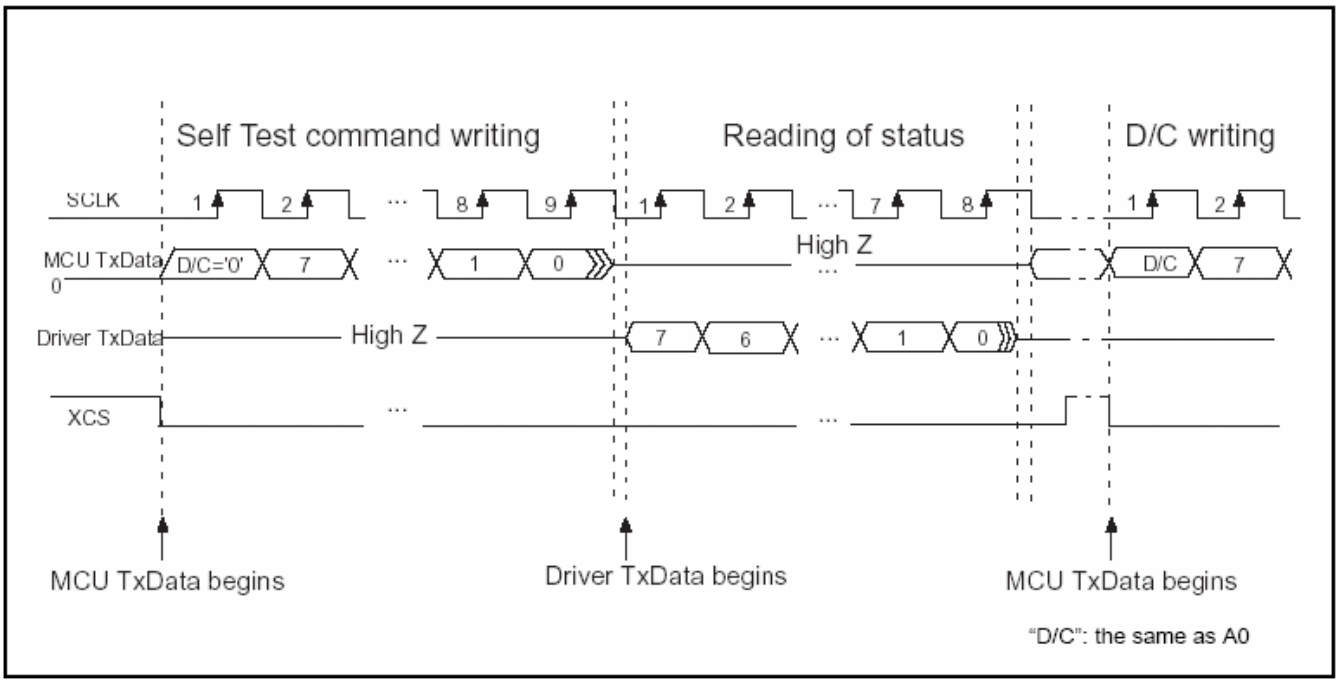
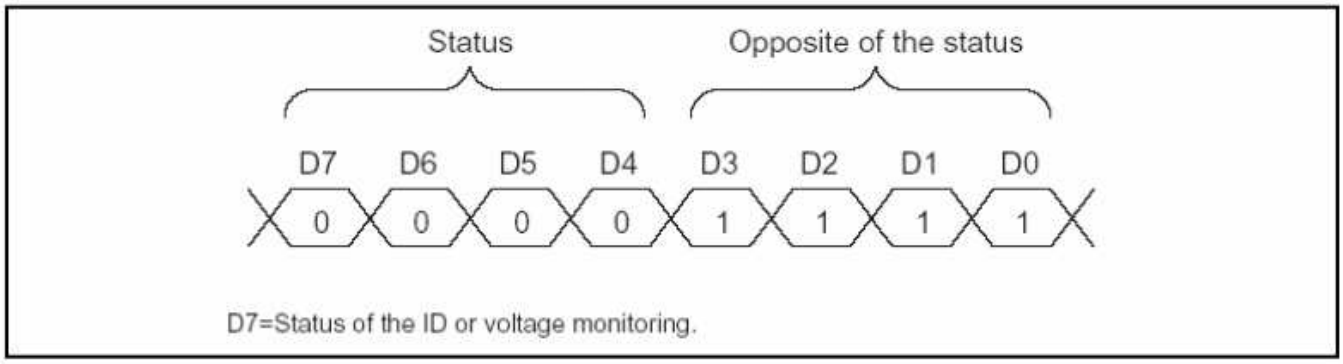


Figure 1-2 shows the timing of reading on one bit of B1….B4

To access Driver TxData-mode a Self Test command is needed to write to driver. The first bit (A0) is low to indicate next 8-bits are for command. The data is read to the driver on the rising edge of SCLK. After last command bit (bit 0) is read SDA-out becomes active (Low impendence) and MCU is able to read data from driver.
The data is read to 8-bit register in MCU so that the bit which was the object of reading is MSB (D7). The same bit value is the written again to the register 3 times in a row by next 3 rising edges of SCLK. These first 4 bits are MSB. The 4 LSB is written to the register as the complement of 4 MSB by 4 next rising edges of SCLK. The complement function is done by the driver.
This function allows to check if the written data is valid.
After written all 8 bits to the register the Auto Return-block in driver release automatically driver back to the MCU TxData-mode, MCU Txdata line changes from high-z to active low in the falling edge of 8th SCLK pulse. CSB must be set high and low again before A0 writing can continue.
SDA-out and SDA-in line can be short circuited in normal working conditions.

Bit No.	D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
Status	0 or 1	Bits have same status as MSB			Bits are complement of 4 MSB (D7~D4)			

For example, if D7 (MSB) has status “0” first 4 bits (D7~D4) represent the status of D7 (“0”) and next four bits (D3~D0) have status “1” because they represent complement data of D7~D4 (see the figure below)
It is recommended to use below 1 MHz SCLK speed for Driver Tx mode (both self test command writing and reading of status). This guarantees that D7 and D6 status bits are also
valid.



PS0= “H” , PS1= “H” , PS2= “H” : I2C Interface

The I2C interface receives and executes the commands sent via the I2C Interface. It also receives RAM data and sends it to the RAM.

The I2C Interface is for bi-directional, two-line communication between different ICs or modules. The two lines are a Serial

Data line (SDA) and a Serial Clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes in the data line at this time will be interpreted as a control signal. Bit transfer is illustrated in Fig.4.

START AND STOP CONDITIONS

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Fig.5.

SYSTEM CONFIGURATION

The system configuration is illustrated in Fig.6.

· Transmitter: the device, which sends the data to the bus

· Receiver: the device, which receives the data from the bus

· Master: the device, which initiates a transfer, generates clock signals and terminates a transfer

· Slave: the device addressed by a master

· Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message

· Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted

· Synchronization: procedure to synchronize the clock signals of two or more devices.

ACKNOWLEDGE

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. A master receiver must also generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the I2C Interface is illustrated in Fig.7.

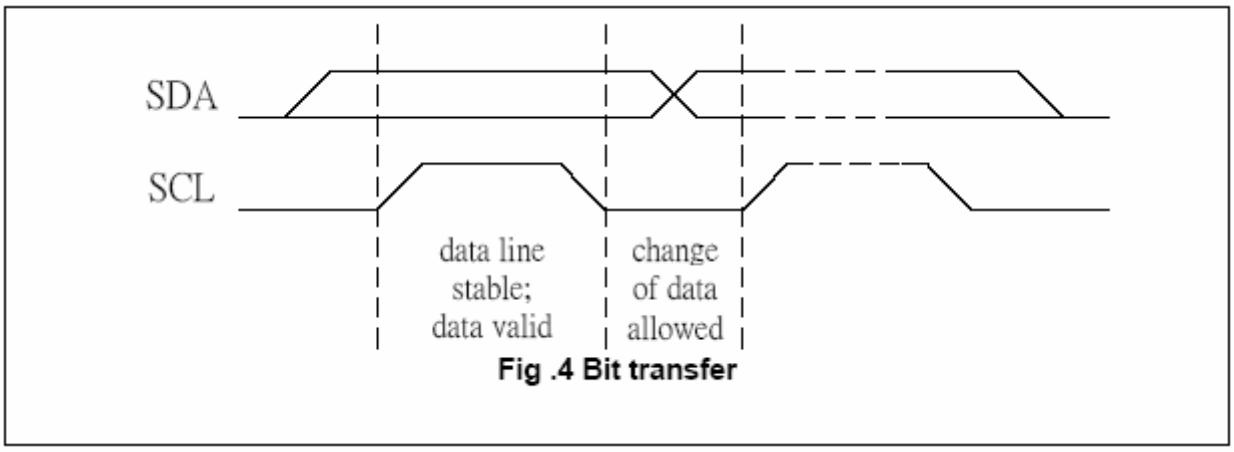


Fig .4 Bit transfer

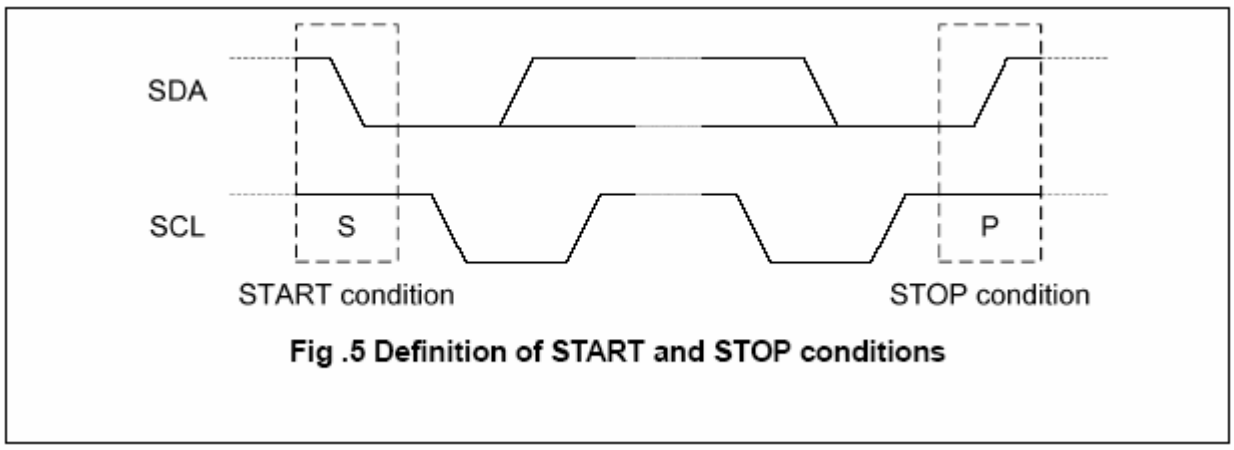


Fig .5 Definition of START and STOP conditions

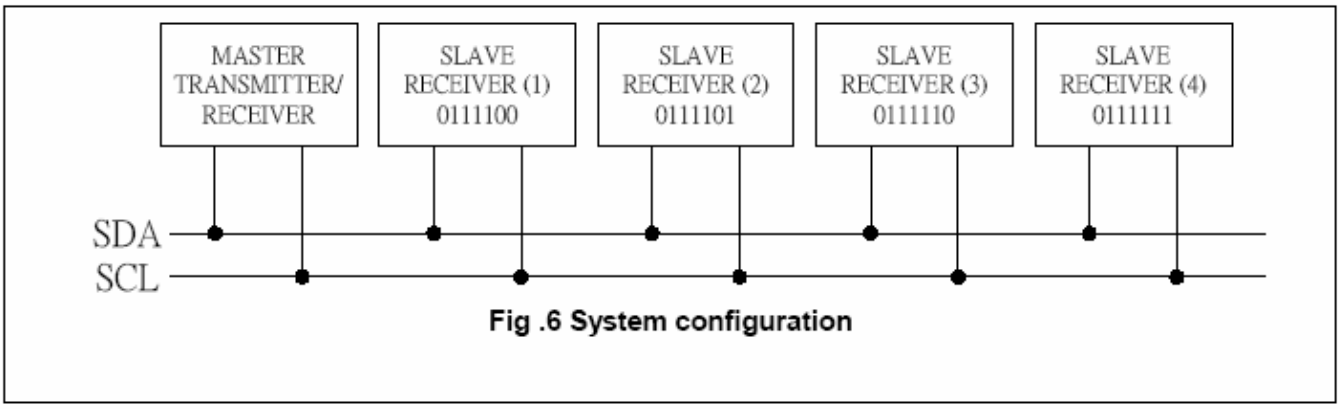


Fig .6 System configuration

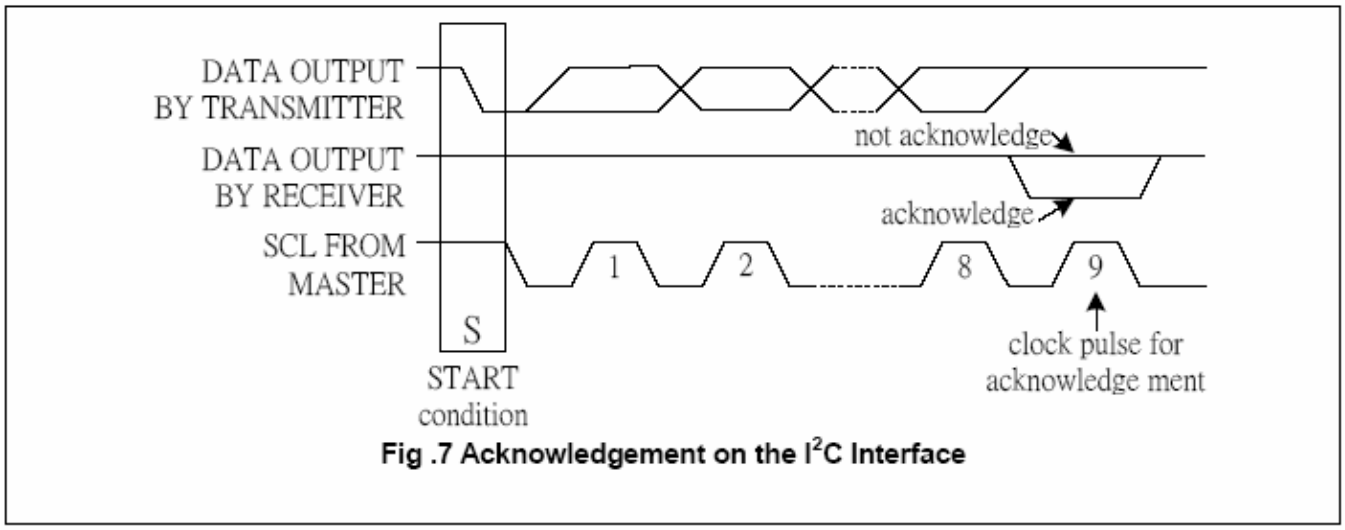


Fig .7 Acknowledgement on the I^2C Interface

I^2C Interface protocol

The ST7549T supports command, data write addressed slaves on the bus.

Before any data is transmitted on the I2C Interface, the device, which should respond, is addressed first. Four 7-bit slave addresses (0111**00**,0111**01**, 0111**10** and 0111**11**) are reserved for the ST7549T. The least significant bit of the slave address is set by connecting the input SA0 and SA1 to either logic 0 (or logic 1 (VDD1).

The I2C Interface protocol is illustrated in Fig.8.

The sequence is initiated with a START condition (S) from the I2C Interface master, which is followed by the slave address.

All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I2C Interface transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves.

A command word consists of a control byte, which defines Co and A0, plus a data byte.

The last control byte is tagged with a cleared most significant bit (i.e. the continuation bit Co). After a control byte with a cleared Co bit, only data bytes will follow. The state of the A0 bit defines whether the data byte is interpreted as a command or as RAM data. All addressed slaves on the bus also acknowledge the control and data bytes. After the last control byte, depending on the A0 bit setting; either a series of display data bytes or command data bytes may follow. If the A0 bit is set to logic 1, these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended ST7549T device. If the A0 bit of the last control byte is set to logic 0, these command bytes will be decoded and the setting of the device will be changed according to the received commands. Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the I2C

INTERFACE-bus master issues a STOP condition (P).If the R/W bit is set to logic 1 the chip will output data immediately after the slave address if the A0 bit, which was sent during the last write access, is set to logic 0. If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.

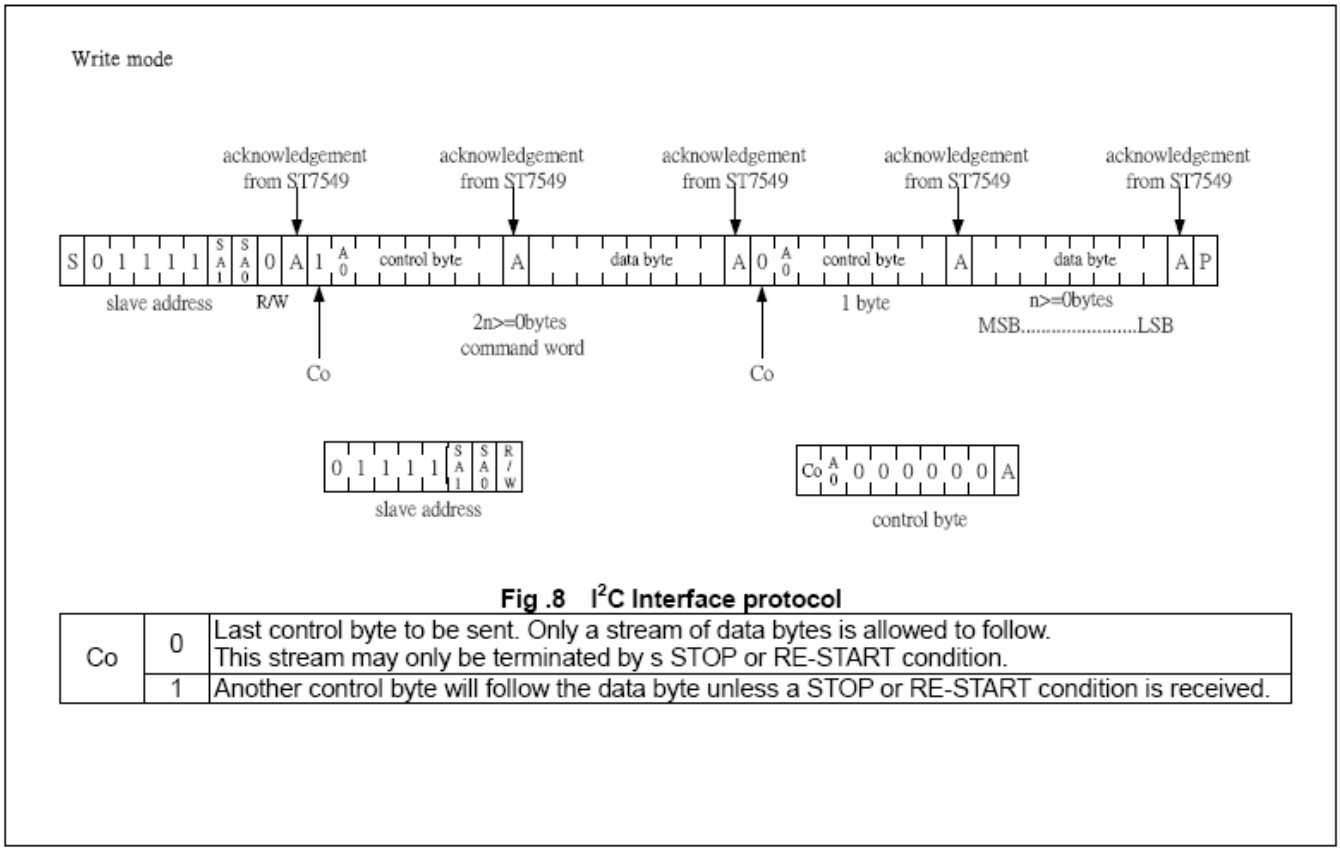


Fig .8 I²C Interface protocol

Co	0	Last control byte to be sent. Only a stream of data bytes is allowed to follow. This stream may only be terminated by s STOP or RE-START condition.
	1	Another control byte will follow the data byte unless a STOP or RE-START condition is received.

Data Transfer

The ST7549T uses bus holder and internal data bus for data transfer with the MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in figure 9. And when reading data from on-chip RAM to the MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in figure 10. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.

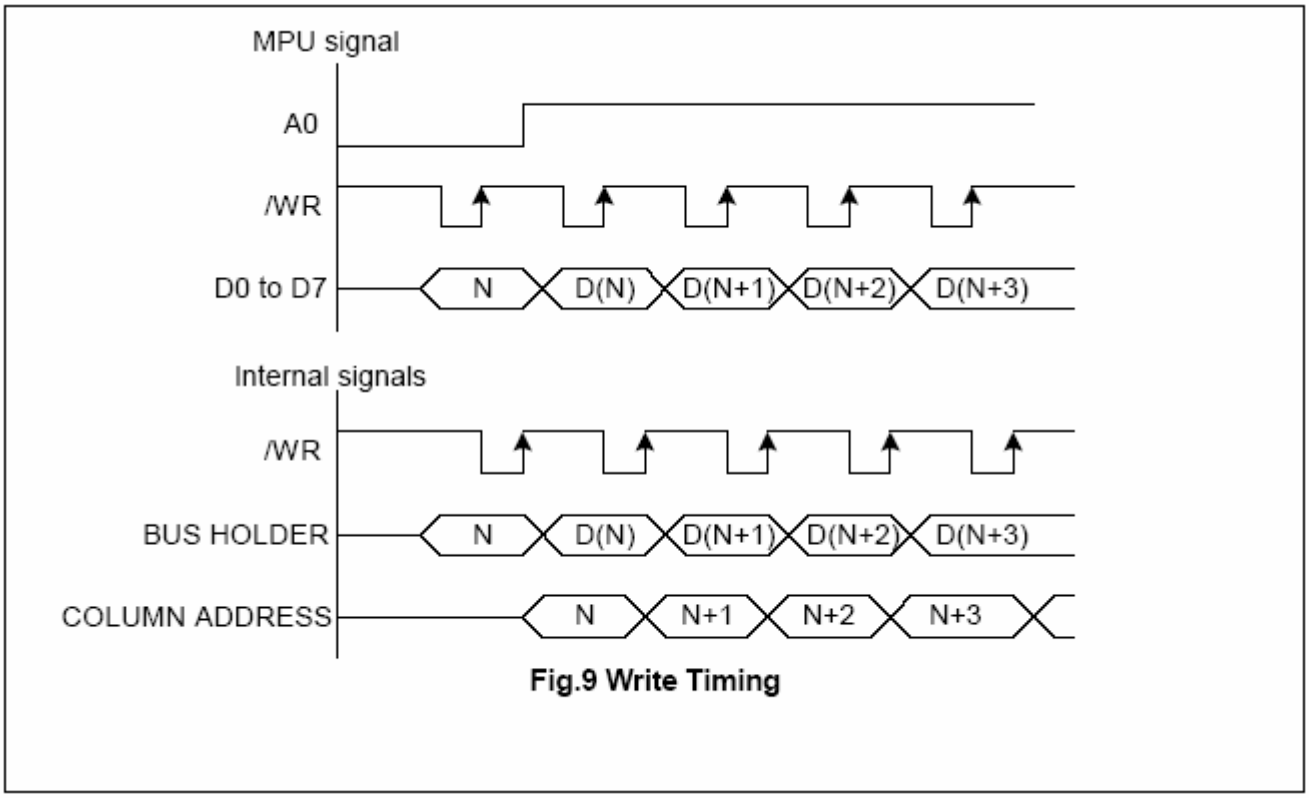


Fig.9 Write Timing

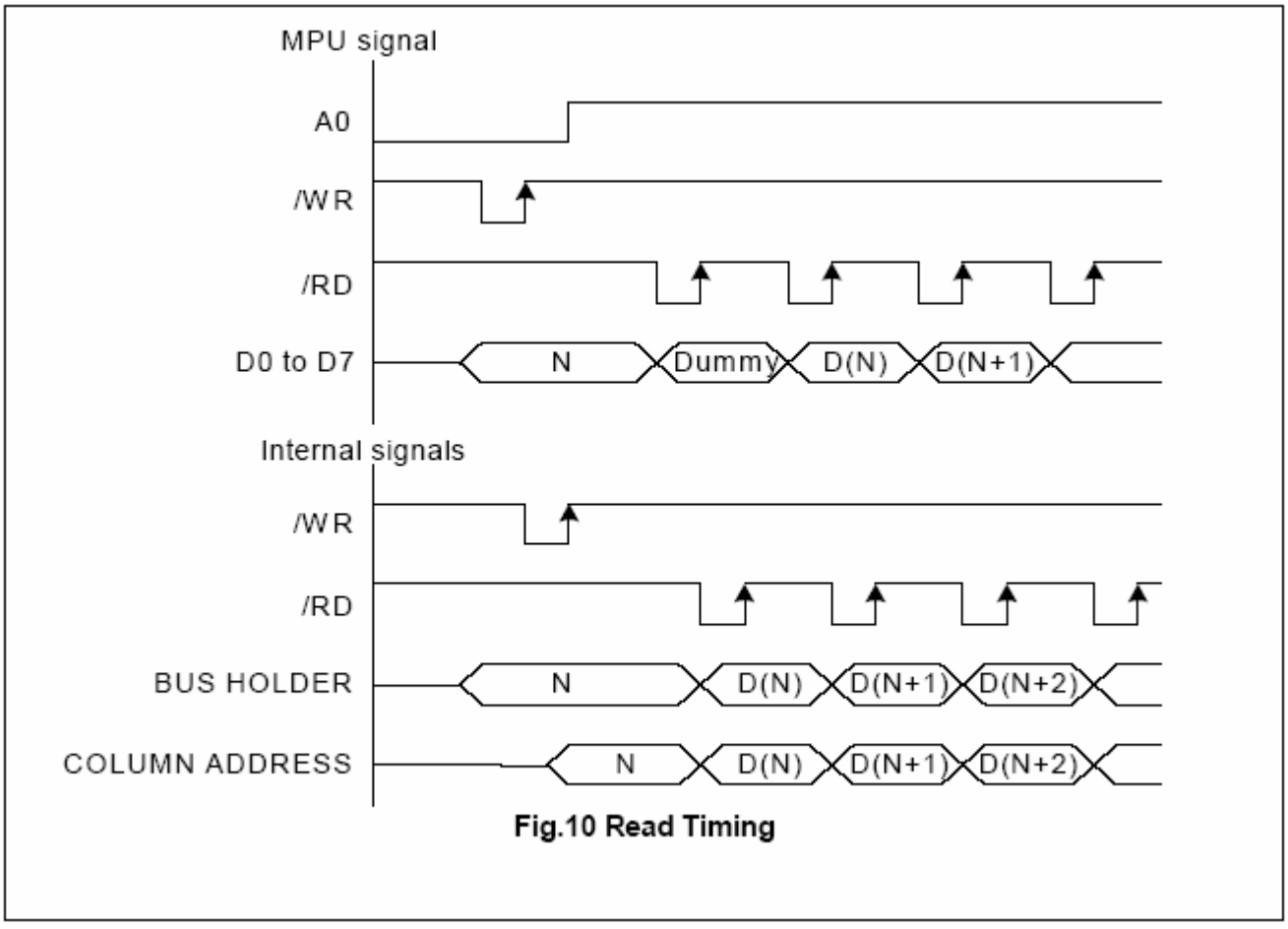


Fig.10 Read Timing

DISPLAY DATA RAM (DDRAM)

The ST7549T contains a 68X102 bit static RAM that stores the display data. The display data RAM store the dot data for the LCD. It has a 68(8 pageX8 bit +1 pageX3 bit +1 pageX1 bit) X 102 . There is a direct correspondence between X-address and column output number. It is 68-row by 102-column addressable array. Each pixel can be selected when the page and column addresses are specified. The 65 rows are divided into 8 pages of 8 lines (0~63 COM) and 8th page with three line (D0 ~D2)(64~ 66 COM) and 9th page with a single line (D0 only)(67 row—COMS (ICON). Data is read from or written to the 8 lines of each page directly through D0 to D7. The display data of D0 to D7 from the microprocessor correspond to the LCD common lines. The microprocessor can read from and write to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into RAM at the same time as data is being displayed without causing the LCD flicker.

Page Address Circuit

This circuit is for providing a Page Address to Display Data RAM. It incorporates 4-bit Page Address register changed by only the “Set Page” instruction. Page Address 9 is a special RAM area for the icons and display data D0 is only valid.

Line Address Circuit

This circuit assigns DDRAM a Line Address corresponding to the first line (COM0) of the display. Therefore, by setting Line
Address repeatedly, it is possible to realize the screen scrolling and page switching without changing the contents of on-chip RAM as shown in figure 10. It incorporates 7-bit Line Address register changed by only the initial display line instruction and 7-bit counter circuit. At the beginning of each LCD frame, the contents of register are copied to the line counter which is increased by CL signal and generates the line address for transferring the 102-bit RAM data to the display data latch circuit. When icon is selected by setting icon page address, display data of icons are not scrolled because the MPU cannot access Line Address of icons.

Column Address Circuit

Column Address Circuit has an 8-bit preset counter that provides Column Address to the Display Data RAM as shown in figure11. The display data RAM column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data read/write command. This allows the MPU display data to be accessed continuously.
Register MX and MY selection instruction makes it possible to invert the relationship between the Column Address and the segment outputs. It is necessary to rewrite the display data on built-in RAM after issuing MX select instruction. Refer to the following figure 12.

SEG Output

SEG Output MX	SEG0 SEG101
“0”	seg0 → Segment Address → seg101
“1”	seg101 ← Segment Address ← seg0

Com Output

SEG Output MY	Com0 Com66	Coms
“0”	com0 → Common Address → com66	Coms
“1”	com66 ← Common Address ← com0	Coms

Duty	MY	Common output pins	
		Com [0:66]	Coms
1/68	0	Com [0:66]	Coms
	1	Com [66:0]	Coms

ADDRESSING

Data is downloaded in bytes into the RAM matrix of ST7549T as indicated in Figs.11, 12, 13, 14. The display RAM has a matrix of 68 by 102 bits. The address pointer addresses the columns. The address ranges are: X 0 to 101 (1100101), Y 0 to 9 (1001) .Addresses outside these ranges are not allowed.
In horizontal addressing mode the X address increments after each byte (see Fig.14). After the last X address (X = 101) X wraps around to 0 and Y increments to address the next row.
After the very last address (X = 101, Y = 9) the address pointers wrap around to address (X = 0, Y =0)

Data structure

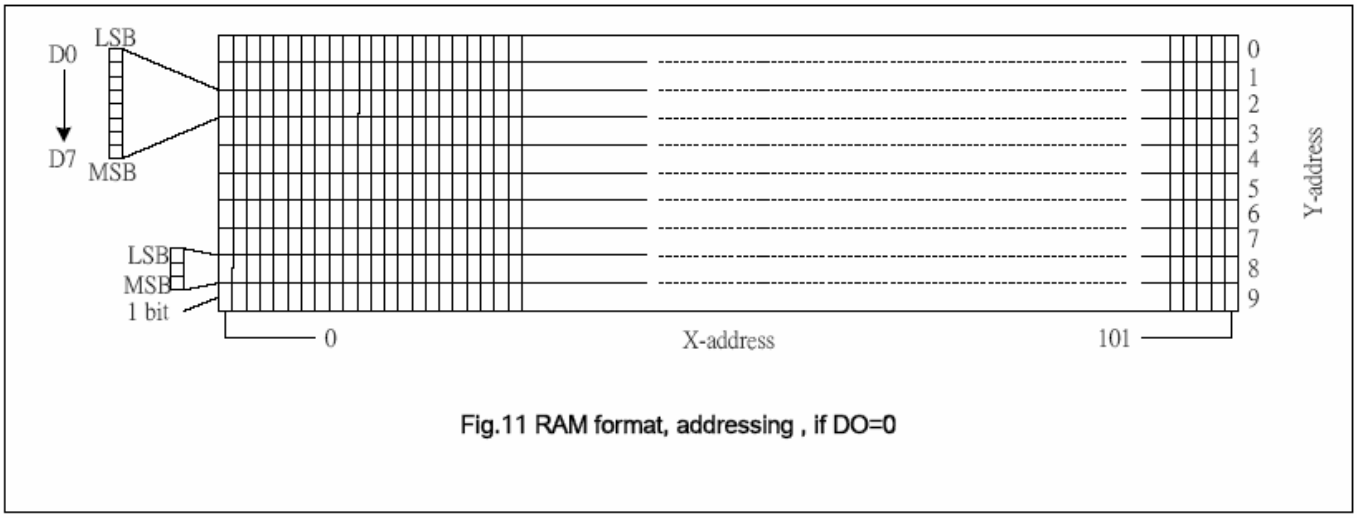


Fig.11 RAM format, addressing , if DO=0

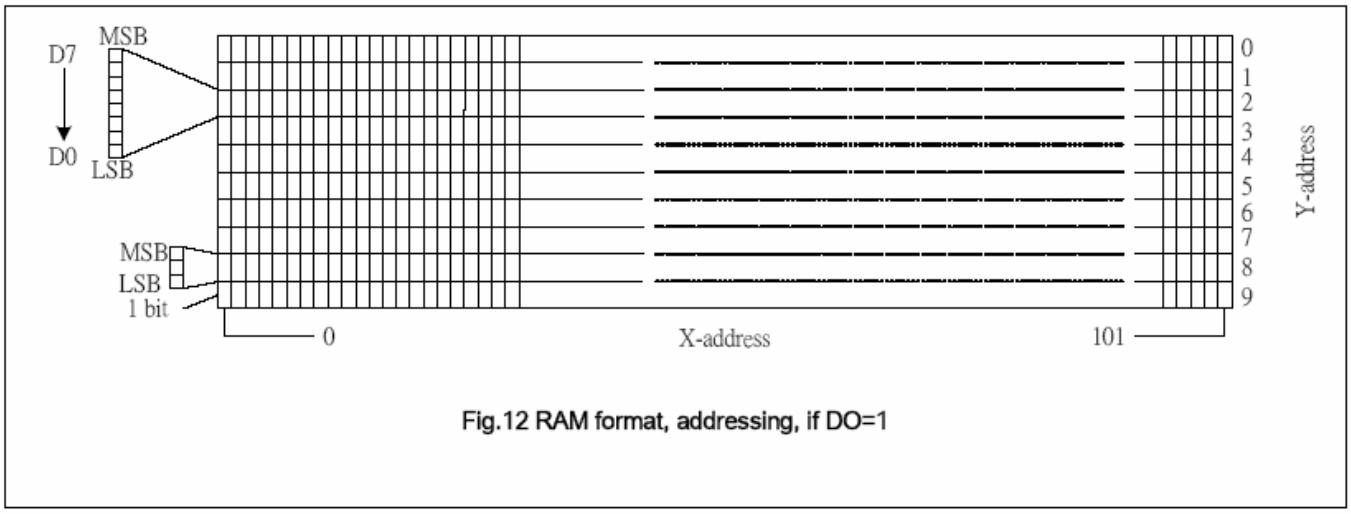


Fig.12 RAM format, addressing, if DO=1

Fig.14 sequence of writing data bytes into RAM with horizontal addressing

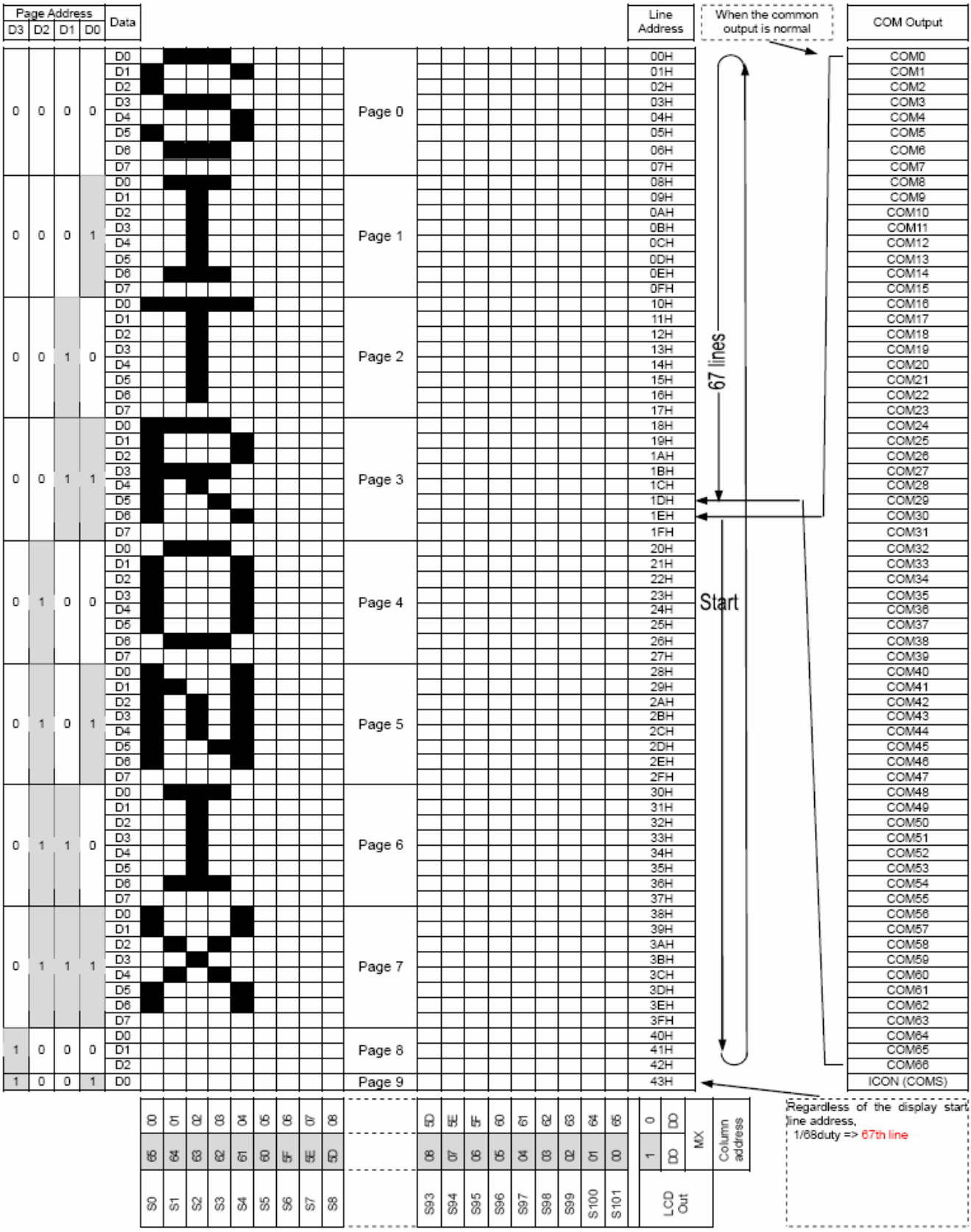


Fig.16 Display Data RAM Map (68 COM)

LCD DRIVER CIRCUIT

68-channel common drivers and 102-channel segment drivers configure this driver circuit. This LCD panel driver voltage depends on the combination of display data and M signal.

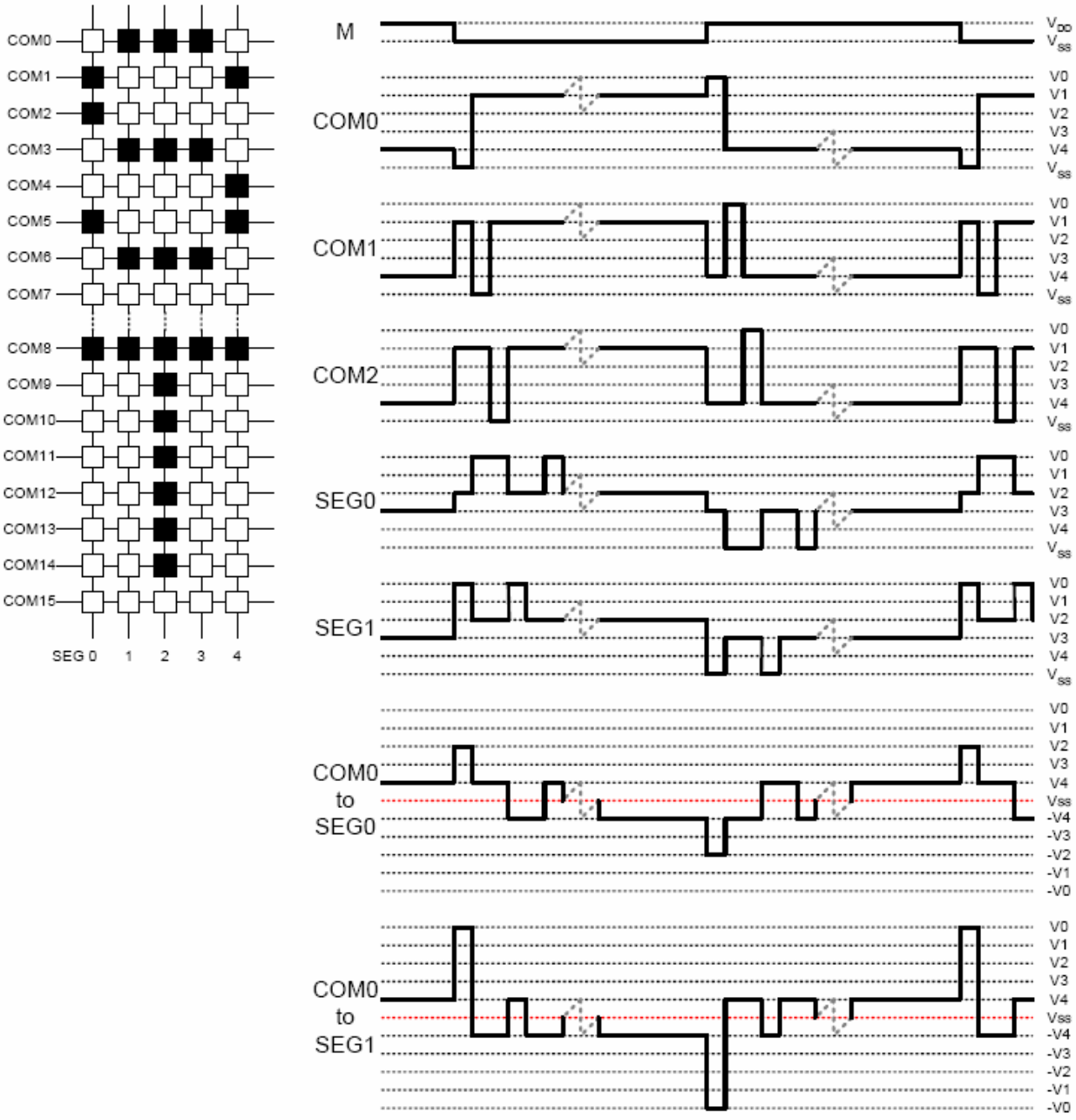


Fig.19 Typical LCD driver waveforms

Partial Display on LCD

The ST7549T realizes the Partial Display function on LCD with low-duty driving for saving power consumption and showing the various display duty. To show the various display duty on LCD, LCD driving duty and bias are programmable via the instruction. And, built-in power supply circuits are controlled by the instruction for adjusting the LCD driving voltages.

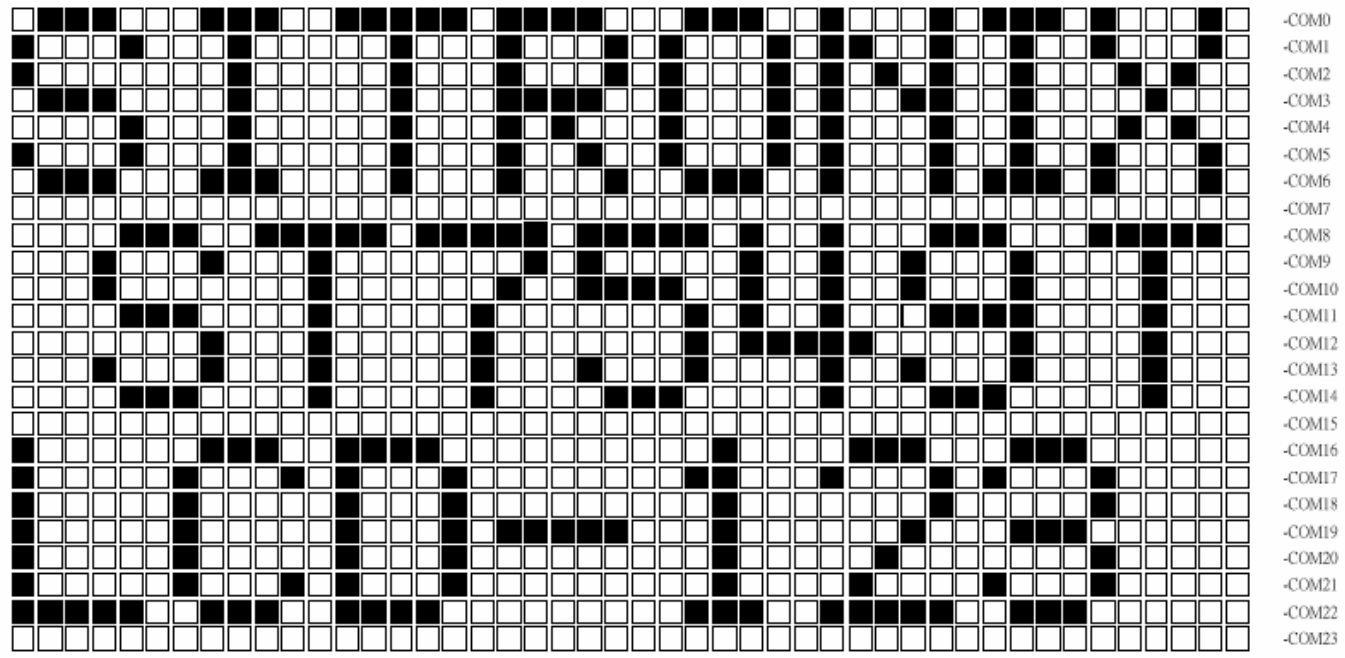


Figure 20.Reference Example for Partial Display

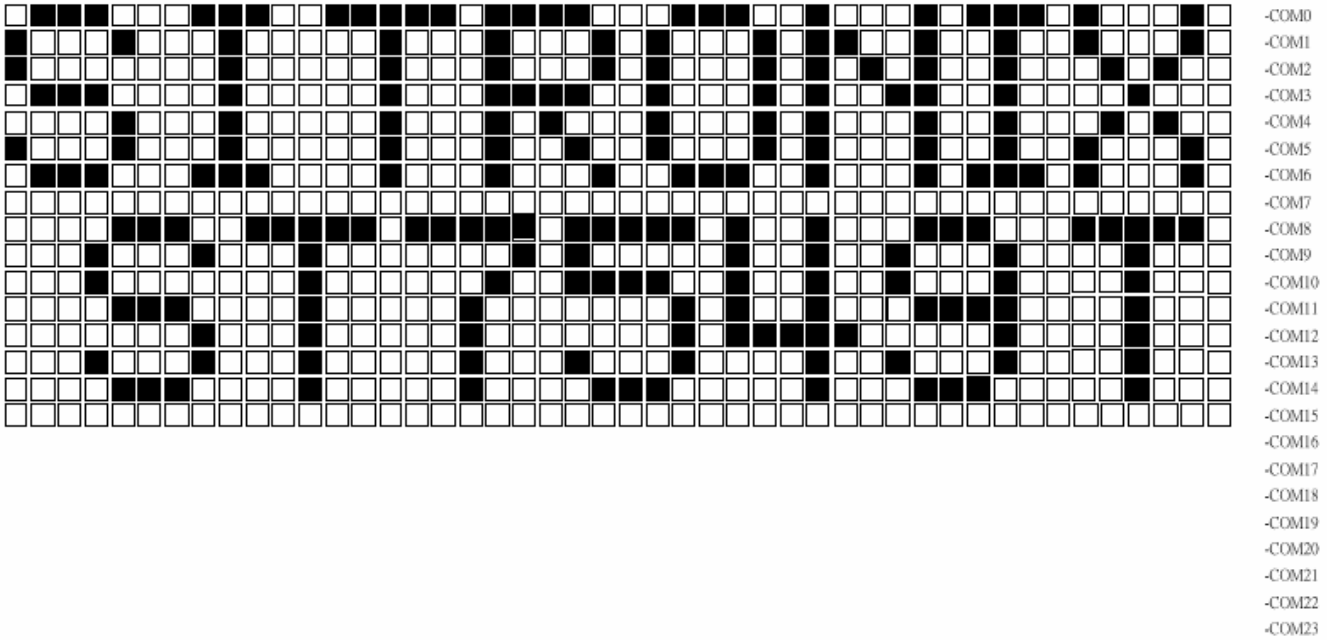


Figure 21.Partial Display (Partial Display Duty=16,initial COM0=0)

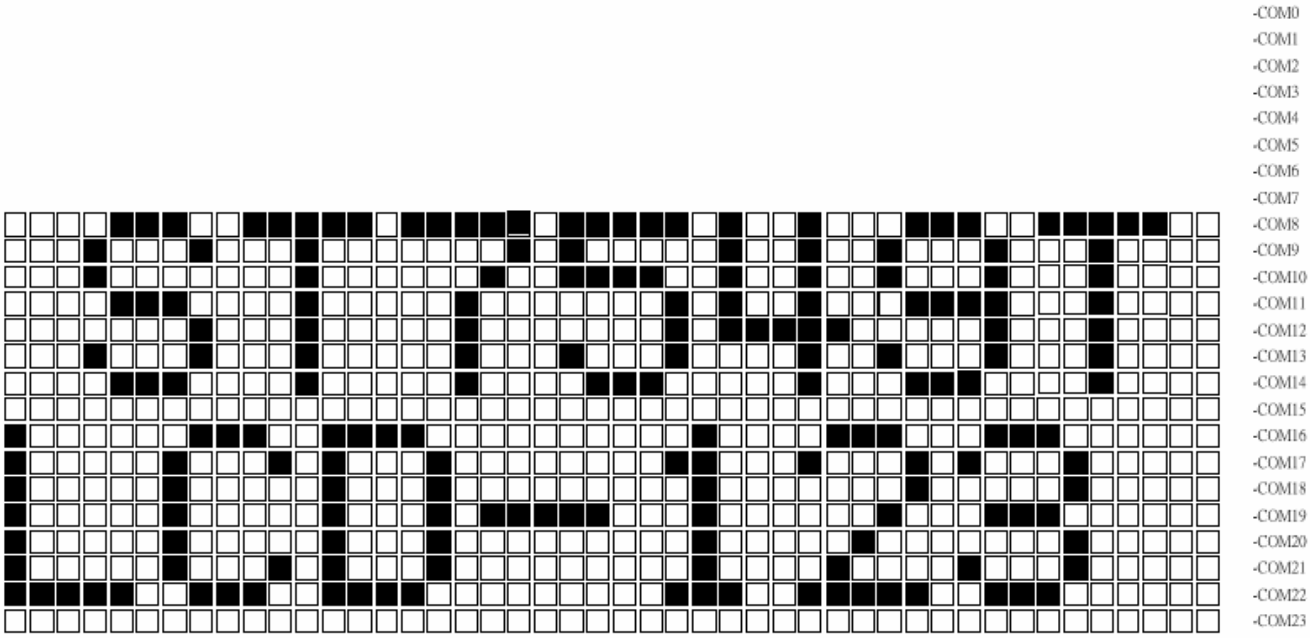


Figure 22.Moving Display (Partial Display Duty=16,Initial COM0=8)

10.RELIABILITY

Content of Reliability Test (wide temperature, -20℃~70℃)

Environmental Test			
Test Item	**Content of Test**	**Test Condition**	**Note**
High Temperature storage	Endurance test applying the high storage temperature for a long time.	80℃ 200hrs	2
Low Temperature storage	Endurance test applying the high storage temperature for a long time.	-30℃ 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70℃ 200hrs	——
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20℃ 200hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60℃,90%RH max For 96hrs under no-load condition excluding the polarizer, Then taking it out and drying it at normal temperature.	60℃,90%RH 96hrs	1,2
Thermal shock resistance	The sample should be allowed stand the following 10 cycles of operation -20℃ 25℃ 70℃ 30min 5min 30min 1 cycle	-20℃/70℃ 10 cycles	——
Vibration test	Endurance test applying the vibration during transportation and using.	Total fixed amplitude : 1.5mm Vibration Frequency : 10~55Hz One cycle 60 seconds to 3 directions of X,Y,Z for Each 15 minutes	3
Static electricity test	Endurance test applying the electric stress to the terminal.	VS=800V,RS=1.5k CS=100pF 1 time	——

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal Temperature and humidity after remove from the test chamber.

Note3: Vibration test will be conducted to the product itself without putting it in a container.

11. Backlight Information

Specification

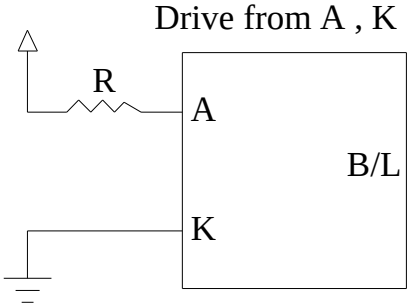
PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITION
Supply Current	ILED	60	75	100	mA	
Supply Voltage	V	3.1	3.2	3.4	V	
Reverse Voltage	VR	—	—	5	V	
Luminous Intensity	IV	547	584	—	CD/M^2	ILED=75mA
Life Time		—	50K	—	Hr.	ILED 75mA
Color	white					

Note: The LED of B/L is drive by current only, drive voltage is for reference only.

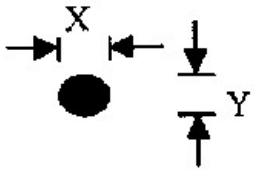
drive voltage can make driving current under safety area (current between minimum and maximum).

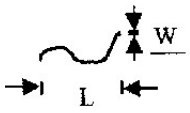
LED B\L Drive Method

Drive from A , K



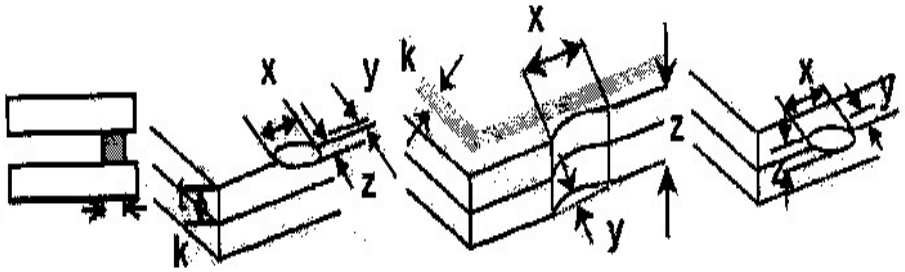
12. Inspection specification

<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>01</td><td>Electrical Testing</td><td>1.1 Missing vertical, horizontal segment, segment contrast defect.
1.2 Missing character , dot or icon.
1.3 Display malfunction.
1.4 No function or no display.
1.5 Current consumption exceeds product specifications.
1.6 LCD viewing angle defect.
1.7 Mixed product types.
1.8 Contrast defect.</td><td>0.65</td></tr>
<tr><td>02</td><td>Black or white spots on LCD (display only)</td><td>2.1 White and black spots on display 0.25mm, no more than three white or black spots present.
2.2 Densely spaced: No more than two spots or lines within 3mm</td><td>2.5</td></tr>
<tr><td rowspan="2">03</td><td rowspan="2">LCD black spots, white spots, contaminati on (non-display)</td><td>3.1 Round type : As following drawing
 

<table>
<tr><td></td><td></td></tr>
<tr><td></td><td></td></tr>
<tr><td></td><td></td></tr>
<tr><td></td><td></td></tr>
<tr><td></td><td></td></tr>
</table></td><td>2.5</td></tr>
<tr><td>3.2 Line type : (As following drawing)
 

<table>
<tr><th>Length</th><th>Width</th><th>Acceptable Q TY</th></tr>
<tr><td>---</td><td>W</td><td>Accept no dense</td></tr>
<tr><td>L</td><td>0.02 W</td><td rowspan="2">2</td></tr>
<tr><td>L</td><td>0.03 W</td></tr>
<tr><td>---</td><td>0.05 W</td><td>As round type</td></tr>
</table></td><td>2.5</td></tr>
<tr><td>04</td><td>Polarizer bubbles</td><td>If bubbles are visible, judge using black spot specifications, not easy to find, must check in specify direction.
<table>
<tr><th>Size</th><th>Acceptable Q TY</th></tr>
<tr><td></td><td>Accept no dense</td></tr>
<tr><td></td><td>3</td></tr>
<tr><td></td><td>2</td></tr>
<tr><td></td><td>0</td></tr>
<tr><td>Total Q TY</td><td>3</td></tr>
</table></td><td>2.5</td></tr>
</table>

<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>05</td><td>Scratches</td><td>Follow NO.3 LCD black spots, white spots, contamination</td><td></td></tr>
<tr><td>06</td><td>Chipped glass</td><td>Symbols Define:
x: Chip length y: Chip width z: Chip thickness
k: Seal width t: Glass thickness a: LCD side length
L: Electrode pad length:

6.1 General glass chip :
6.1.1 Chip on panel surface and crack between panels:
 

<table>
<tr><td>C</td><td>C</td><td>C</td></tr>
<tr><td></td><td></td><td></td></tr>
<tr><td></td><td></td><td></td></tr>
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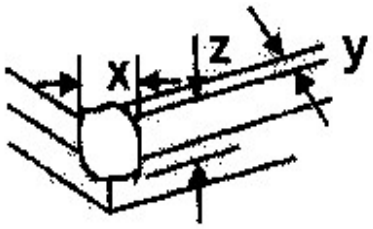
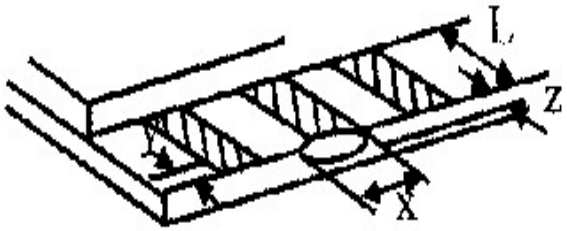
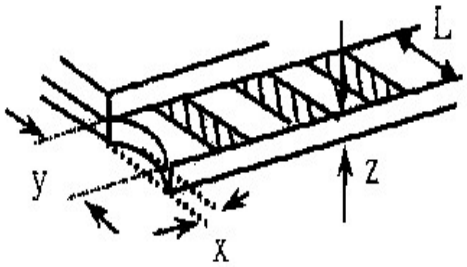
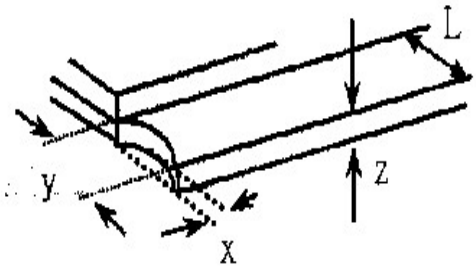
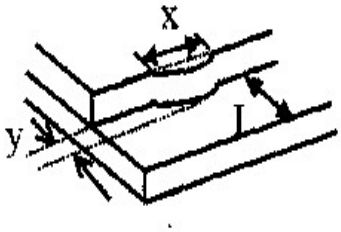
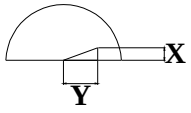
C
 

<table>
<tr><td>C</td><td>C</td><td>C</td></tr>
<tr><td></td><td></td><td></td></tr>
<tr><td></td><td></td><td></td></tr>
</table></td><td>2.5</td></tr>
</table>

NO	Item	Criterion	AQL
06	Glass crack	x: Chip length y: Chip width z: Chip thickness k: Seal width t: Glass thickness a: LCD side length L: Electrode pad length 6.2 Protrusion over terminal : 6.2.1 Chip on electrode pad :  C C C   C C C L  L	2.5

NO	Item	Criterion	AQL
07	Cracked glass	LCD	2.5
08	Backlight elements	LCD	0.65 2.5 0.65
09	Bezel		2.5 0.65
10	PCB COB	C C C The height of the COB should not exceed the height indicated in the assembly diagram. 10.4 There may not be more than 2mm of sealant outside the seal area on the PCB. And there should be no more than three places. 10.5 No oxidation or contamination PCB terminals. 10.6 Parts on PCB must be the same as on the production characteristic chart. There should be no wrong parts, missing parts or excess parts. 10.7 The jumper on the PCB should conform to the product characteristic chart. 10.8 If solder gets on bezel tab pads, LED pad, zebra pad or screw hold pad, make sure it is smoothed down. The Scraping testing standard for Copper Coating of PCB  **X * Y<=2mm^2**	2.5 2.5 0.65 2.5 2.5 0.65 0.65 2.5 2.5
11	Soldering	C C C	2.5 2.5 2.5 0.65

NO	Item	Criterion	AQL
12	General appearance		2.5
		L C	
		L C	0.65
			2.5
		C C	2.5
			2.5
			2.5
			2.5
			0.65
			0.65
		LCD	0.65
			0.65

13. Material List of Components for RoHs

1. WINSTAR Display Co., Ltd hereby declares that all of or part of products (with the mark "#"in code), including, but not limited to, the LCM, accessories or packages, manufactured and/or delivered to your company (including your subsidiaries and affiliated company) directly or indirectly by our company (including our subsidiaries or affiliated companies) do not intentionally contain any of the substances listed in all applicable EU directives and regulations, including the following substances.

Exhibit A：The Harmful Material List

Material	(Cd)	(Pb)	(Hg)	(Cr6+)	PBBs	PBDEs
Limited Value	100 ppm	1000 ppm	1000 ppm	1000 ppm	1000 ppm	1000 ppm
Above limited value is set up according to RoHS.						

2.Process for RoHS requirement：

(1) Use the Sn/Ag/Cu soldering surface the surface of Pb-free solder is rougher than we used before.

(2) Heat-resistance temp.：

Reflow：250℃,30 seconds Max.

Connector soldering wave or hand soldering：320℃, 10 seconds max.

(3) Temp. curve of reflow, max. Temp.：235±5℃

Recommended customer's soldering temp. of connector：280℃, 3 seconds.

winstar **LCM Sample Estimate Feedback Sheet**

Module Number：_____ **Page: 1**

1 Panel Specification：

1.	Panel Type：	Pass	NG ,_____
2.	View Direction：	Pass	NG ,_____
3.	Numbers of Dots：	Pass	NG ,_____
4.	View Area：	Pass	NG ,_____
5.	Active Area：	Pass	NG ,_____
6.	Operating Temperature：	Pass	NG ,_____
7.	Storage Temperature：	Pass	NG ,_____
8.	Others：_____		

2 Mechanical Specification：

1.	PCB Size：	Pass	NG ,_____
2.	Frame Size：	Pass	NG ,_____
3.	Materal of Frame：	Pass	NG ,_____
4.	Connector Position：	Pass	NG ,_____
5.	Fix Hole Position：	Pass	NG ,_____
6.	Backlight Position：	Pass	NG ,_____
7.	Thickness of PCB：	Pass	NG ,_____
8.	Height of Frame to PCB：	Pass	NG ,_____
9.	Height of Module：	Pass	NG ,_____
10.	Others：	Pass	NG ,_____

3 Relative Hole Size：

1.	Pitch of Connector：	Pass	NG ,_____
2.	Hole size of Connector：	Pass	NG ,_____
3.	Mounting Hole size：	Pass	NG ,_____
4.	Mounting Hole Type：	Pass	NG ,_____
5.	Others：	Pass	NG ,_____

4 Backlight Specification：

1.	B/L Type：	Pass	NG ,_____
2.	B/L Color：	Pass	NG ,_____
3.	B/L Driving Voltage (Reference for LED Type)：	Pass	NG ,_____
4.	B/L Driving Current：	Pass	NG ,_____
5.	Brightness of B/L：	Pass	NG ,_____
6.	B/L Solder Method：	Pass	NG ,_____
7.	Others：	Pass	NG ,_____

Go to page 2

5 Electronic Characteristics of Module：

1.	Input Voltage：	Pass	NG ,_____
2.	Supply Current：	Pass	NG ,_____
3.	Driving Voltage for LCD：	Pass	NG ,_____
4.	Contrast for LCD：	Pass	NG ,_____
5.	B/L Driving Method：	Pass	NG ,_____
6.	Negative Voltage Output：	Pass	NG ,_____
7.	Interface Function：	Pass	NG ,_____
8.	LCD Uniformity：	Pass	NG ,_____
9.	ESD test：	Pass	NG ,_____
10.	Others：	Pass	NG ,_____

6 Summary：

Sales signature：_____

Customer Signature：_____ **Date**： / /